Voice-Switched Circuit for Handsfree Operation

Description

The voice switched speakerphone integrated circuit, U4080B, incorporates a variety of functions (see below). The versality of the device is further enhanced by the provision of a large number of pins giving access to internal circuit points.

Features

- Operates on telephone lines, integrated reference voltage regulation
- Output power: 100 mW at a 25-Ω load with peak limitation
- Chip select pin for active/standby operation
- Linear volume control
- Monitoring system for background sound level
- Wide operating dynamic range through signal compression

Block Diagram / Application Circuit

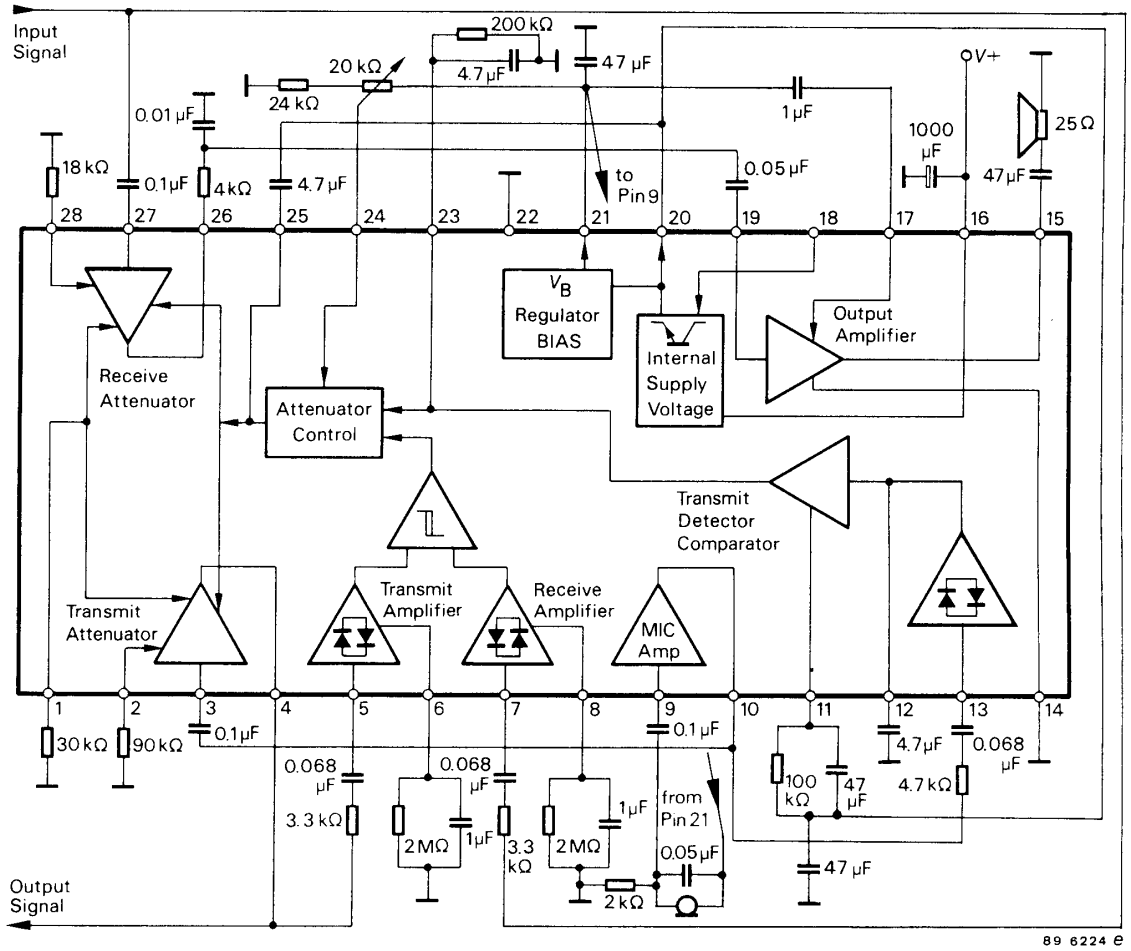


Figure 1. Block diagram and application circuit

Pin Description

Pin	Symbol	Function
1	R1	Load resistance. Provides reference current for the transmit and receive attenuators.
2	RTG	Transmit attenuator nominal gain resistor. Transmit channel gain is inversely proportional to the resistance RTG connected to Pin 2.
3	TI	Transmit attenuator input. Input resistance is 5 kΩ
4	TO	Transmit attenuator output. Drives the input of the transmit level detector and the external circuit which drives the telephone line.
5	TLI	Transmit level detector input. Sets the detector level. Sensitivity to transmit channel signals increases when the value of the resistor decreases.
6	TLO	Transmit level detector output. The external RC-element sets the time the comparator will hold the system in the transmit mode after speech ceases.
7	RLI	Receive level detector input. An external resistance connected to the pin sets the detection level. Sensitivity to receive channel signals increases when the resistor decreases.
8	RLO	Receive level detector output. RC-element connected at the pin sets the time the comparator will hold the system in the receive mode after the receive signal expires.
9	MIC	Microphone amplifier input. Input impedance is 10 kΩ and the bias voltage is approximately equal to $V_{B.}$
10	MICO	Microphone amplifier output. Gain is set internally at 34 dB (50 V/V).
11	CP1	RC circuit for holding background noise level. The transmit detector compares the CP1 voltage with the speech signal from CP2.
12	CP2	Capacitor for detecting the speech signal for comparison with the background noise held at Pin 11 (CP1).
13	TDI	Transmit detector input. The microphone amplifier output is coupled to the TDI pin through an external resistor.

Pin	Symbol	Function
14	GND1	High current ground pin for the speaker amplifier output stage. GND1 voltage should be within 10 mV of the ground voltage of Pin 22.
15	SAO	Speaker amplifier output. It will source and sink up to 100 mA when ac coupled to the speaker. Gain is set internally at 34 dB (50 V/V).
16	V+	DC supply.
17	AGC	A capacitor from this pin to V_B stabilizes the speaker amplifier gain control loop, and additionally controls the attack and decay time of this circuit. The gain control loop limits the speaker amp input to prevent clipping at SAO. The internal resistance at the AGC pin is nominally 110 kΩ.
18	CS	Digital chip select input. Logic O: VCC regulator is enabled when ≦ 0.7 V; Logic 1: Standby mode drawing 0.5 mA when ≧ 1.6 V
19	SAI	Speaker amplifier input. Input impedance is ca. 20 kΩ.
20	VCC	Regulated output voltage (5.4 V). It powers all circuits except the speaker amplifier output. This voltage can be used for an external circuit i.e., a microprocessor where a filter capacitor is required.
21	V_B	Output voltage. V_B is approximately VCC/2 and serves as an analog ground to the speaker-phone system.
22	GND2	Integrated circuit ground (except for the speaker amplifier).
23	TDO	Transmit detector output. An external RC circuit holds the system in the transmit mode during pauses between words or phrases.
24	VCI	Volume control input. A variable resistor connected to this pin provides receive mode volume control.
25	ACF	Attenuator control filter. A connected capacitor reduces noise transients as the attenuator control switches levels of attenuation.

Pin	Symbol	Function
26	RECO	Receive output attenuator. This pin is normally ac coupled to the input of the speaker amplifier (Pin 19 – SAI)
27	RECI	Receive input attenuator. Input resistance is nominally 5 kΩ.
28	RG	Resistor connected from Pin 28 to ground determines the nominal gain of the receive attenuator. The receive channel gain is directly proportional to the RG resistance.

Absolute Maximum Ratings

Reference point Pin 22, T_{amb} = 25°C, unless otherwise specified

Parameters		Symbol	Value	Unit
Supply voltage	Pin 16	V+	14	V
Digital chip select input voltage	Pin 18	V_{18}	14	V
Speaker amplifier ground voltage	Pin 14	V_{14}	3	V
Volume control input voltage	Pin 24	V_{24}	V_{CC}	°C
Storage temperature range		T_{stg}	−40 to +125	°C
Junction temperature		T_j	125	°C
Ambient temperature range		T_{amb}	−20 to +60	
Power dissipation T_{amb} = 60°C		P_{tot}	1.3	W

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	50	K/W

Electrical Characteristics

V_{16} = +7.5 V, V_{18} = 0.7 V, figure 1, T_{amb} = 25°C, unless other specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltages						
Supply current V_{16} = 11 V, V_{18} = 0.7 V V_{16} = 11 V, V_{18} = 1.6 V	 Pin 16 Pin 16	 I+ I+			 9.0 800	mA
Regulated output voltage	Pin 20	V_{CC}	4.9	5.4	5.9	V
Line regulation (deviation) 6.5 V ≦ V_I ≦ 11 V		ΔV_{CC}		65	150	mV
Output resistance I_{CC} = 3 mA		R_O		6.0	20	Ω
Dropout voltage V_{16} = 5 V		V_{CCSat}		80	300	mV
Output voltage	Pin 21	V_B	2.5	2.9	3.3	V
Output resistance I_B = 1.7 mA	Pin 21	R_O		250		Ω
Attenuators						
Receive attenuator gain f = 1 kHz, R_{mode}, $V_{24} = V_B$ V_{27} = 250 mV_{rms}	Pin 26, 27	G_R	2.0	6.0	10	dB
Gain range R to T modes		ΔG_R	40	44	48	dB
Idle mode, V_{27} = 250 V_{rms}		G_{RI}	–20	–16	–12	dB
RECO voltage (R mode)		V_{RECO}	1.8	2.3	3.2	V
Delta RECO voltage		ΔV_{RECO}			100	mV
RECO sink current (R mode)		I_{RECOL}	75			µA
RECO source current (R mode)		I_{RECOH}	1.0		3.0	mA
RECI input resistance		R_{RECI}	3.5	5.0	8.0	kΩ
Volume control range (R attenuator gain, R mode) 0.6 V_B ≦ V24 ≦ V_B		V_{CR}	24.5	22.5	32.5	dB
Transmit attenuator gain	**Pins 3 and 4**					
f = 1 kHz, T_{mode}, V_3 = 250 mV_{rms}		G_T	4.0	6.0	8.0	dB
Gain range T to R mode		ΔG_T	40	44	48	dB
Idle mode, V_3 = 250 mV_{rms}		G_{TI}	–16.5	–13	–8.5	dB
TO voltage (T mode)		V_{TO}	1.8	2.3	3.2	V
Delta TO voltage switch from T to R mode		ΔV_{TO}			100	mV
TO sink current, T mode		I_{TOL}	75			µA
TO source current, T mode		I_{TOH}	1.0		3.0	mA
TI input resistance		R_{TI}	3.5	5.0	8.0	kΩ

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Speaker amplifier	**Pins 15 and 19**					
Gain, V_{19} = 20 mV_{rms}		G_{SA}	33	34	35	dB
Input impedance		R_I	15	22	37	kΩ
Output voltage (Pin 19 = cap coupled to GND)		V_O	2.4	3.0	3.6	V
High output voltage V_{19} = 0.1 V, V_{15} = –100 mA		V_{OH}	5.5			V
Low output voltage V_{19} = –0.1 V, V_{15} = +100 mA		V_{OL}			600	mA
Log amplifiers						
Receive level detector leakage current $V_8 = V_B$ + 1.0 V	Pin 8	I_{LR}			2.0	µA
Transmit level detector leakage current $V_6 = V_B$ + 1.0 V	Pin 6	I_{LT}			2.0	µA
Transmit-Receive switching threshold V_8/V_6 at 20 µA to switch	Pins 5 and 7					
T-R comparator	Pin 25	I_{TH}	0.8		1.2	
Transmit detector	**Pin 23**					
DC voltage: Idle mode T mode		V_{23} V_{23}		0 4.0		V
Distortion	Pins 15 and 27					
R mode: RECI to SAO V_{27} = 10 mV_{rms}, f = 1 kHz		d		1.5		%
T mode: MIC to TO V_9 = 5 mV_{rms}, f = 1 kHz		d		2.0		%

Transmit and Receive Attenuators

The transmit and receive attenuators are supplementary in function. This means that when one is at maximum gain, the other is at maximum attenuation, and vice versa. That is, both are never on or off. They are controlled by the voltage of ACF (attenuator control filter) at Pin 25 being supplied by attenuator control as shown in figure 1 The ACF voltage is provided by the attenuator control block, which receives the three inputs given below:

- R-T comparator
- Transmit detector comparator
- Volume control

The response of the attenuators is based on the difference between the ACF voltage and V_{CC}. If the difference (ΔV_{ACF}) is ≈ 6 mV, the transmit attenuator is fully on and the receive attenuator is fully off (T mode). If ΔV_{ACF} ≈ 150 mV, the circuit is in the R mode. If ΔV_{ACF} ≈ 75 mV, the circuit is in the idle mode, and the two attenuators are at gain settings approximately half way (in dB) between their fully on and fully off positions.

Three resistors R_1, RTG and RD, determine maximum gain and attenuation values. R_1 effects both attenuators according to its value relative to RTG and RG. Figure 4 shows the variations versus the ratio of other resistors to R1. RTG affects the gain and attenuation of only the transmit attenuator according to the curves of figure 2, while RG affects only the receive attenuator according to figure 3 Gain difference from on to off, according to the figures, is a reasonably constant 45 dB until the upper gain limit is approached. A value of R1 = 30 kΩ is recommended as a starting point, and then the values of RTG and RG selected to suit the particular design goals.

The input impedance of the attenuators (at TI and RECI) is typically 5.0 kΩ, and the maximum input signal which will not cause output distortion is 250 mV_{rms} (707 mV_{pp}). The 4 kΩ resistor and 0.01 µF capacitor at RECO (in figure 1) filters out high-frequency components in the receive path. This helps to minimize high-frequency acoustic feedback problems which may occur if the filter were not present.

The filter's insertion loss is 1.5 dB at 1.0 kHz. The outputs of the attenuators are inverted from their inputs. Referring to the attenuator control block, the ΔV_{ACF} voltage at its output is determined by three inputs. The relationship of the inputs and outputs is summarized in the following truth table:

T-R Comp	Transmit Det Comp	Volume Control	ΔV_{ACF}	Mode
Transmit	Transmit	No Effect	6.0 mV	Transmit
Transmit	Idle	No Effect	75.0 mV	Idle
Receive	Transmit	Affects ΔV_{ACF}	50 – 150 mV	Receive
Receive	Idle	Affects ΔV_{ACF}	50 – 150 mV	Receive

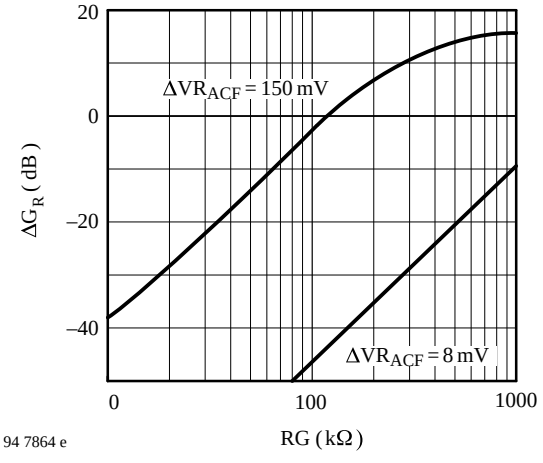


Figure 2.

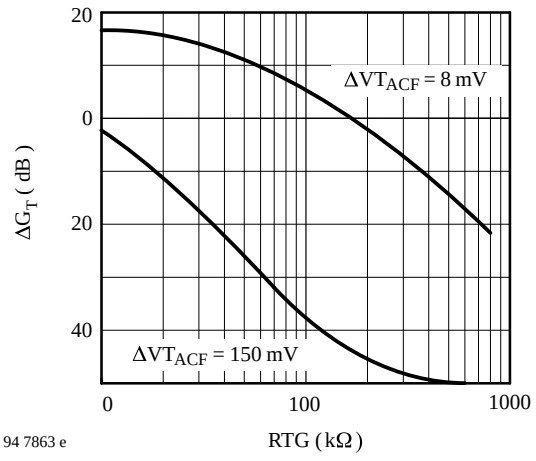


Figure 3.

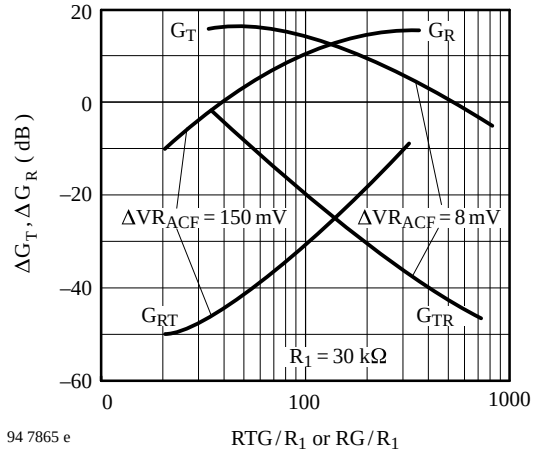


Figure 4.

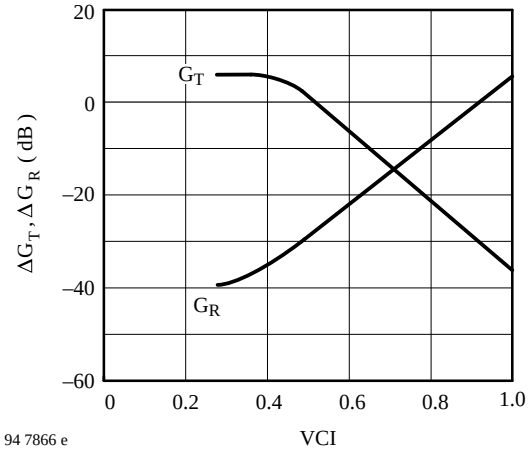


Figure 5.

As can be seen from the truth table, the T-R comparator dominates. The transmit detector comparator is effective only in the transmit mode, and the volume control is effective only in the receive mode. The T-R comparator is in the transmit position when the transmit signal present is greater than the receive signal. The transmit detector comparator then determines whether the transmit signal is a result of background noise (a relatively constant signal), or speech, which consists of bursts. If the signal is due to background noise, the attenuators will be put into the idle mode (ΔV_{ACF} = 75 mV). If the signal consists of speech, the attenuators will be switched to the transmit mode (ΔV_{ACF} = 6.0 mV). For further explanation, please refer to the transmit detector circuit (Log. amplifiers).

The T-R comparator is in the receive position when there is sufficient receive signal to overcome the background noise AND any speech signals. The ΔV_{ACF} voltage will be 150 mV if the volume control is at the maximum position, i.e. VCI (Pin 24) = V_B. If VCI $\leqq V_{B'}$, RG and TG will vary in a complementary manner as shown in figure 5 It can be seen that at the minimum recommended operating level (VCI = 0.55 V_B) the gain of the transmit attenuator is actually greater than that of the receive attenuator. The effect of varying VCI is to vary ΔV_{ACF}, with a resulting variation in the gains of the attenuators. Figure 6 shows the gain variations with ΔV_{ACF}.

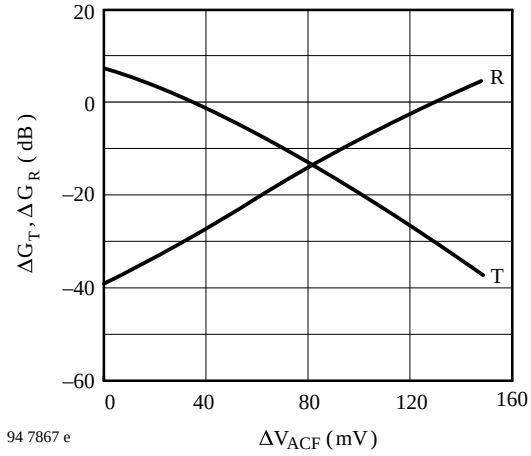


Figure 6.

A 4.7 µF capacitor at Pin 25 smooths the transition between operating modes. This keeps down any “clicks” in the speaker or transmit signal when the ACF voltage switches. The gain separation of the two attenuators can be reduced from the typical 45 dB by connecting a resistor between Pins 20 and 25. The effect is a reduction of voltage in the receive mode, but no effect on the transmit mode voltage.

For example, adding a 12 kΩ resistor will reduce ΔV_{ACF} by approximately 15 mV (to 135 mV), decrease the gain of the receive attenuator by approximately 5.0 dB, and increase the gain of the transmit attenuator by a similar amount. If the circuit requires the receive attenuator gain to be +6.0 dB in the receive mode, RG must be adjusted (to 27 kΩ) to re-establish this value. This change will also increase the receive attenuator’s gain in the transmit mode by a similar amount. The resistor at TLI may also require changing to reset the sensitivity of the transmit level detector.

Log Amplifiers (Transmit and Receive Level Detectors)

The log amplifiers monitor the levels of the transmit and receive signals so as to tell the I-R comparator which mode is in operation. The input signals are applied to the amplifiers (at TLI and RLI) through coupling capacitors and current limiting resistors.

The value of these components determines the sensitivity of the respective amplifiers and has an effect on the switching times between transmit and receive modes.

The feedback elements for the amplifiers are back-to-back diodes which provide a logarithmic gain curve, thus allowing the operation over a wide range of signal levels. The output of the amplifiers are rectified, having a fast rise time and a slow decay time. The rise time ($\leqq$ 1 ms) is determined by the capacitor at Pin 6 (or Pin 8) and an internal 500 Ω resistor.

The decay time ($\leqq$ 1 s) is determined by the external RC values at Pin 7. The switching time is not fixed, but depends on the relative values of the transmit and receive signals, as well as these external components. Figure 7 indicates the dc transfer characteristics of the log amps, and figure 8 indicates the transfer characteristics with respect to an ac input signal. The dc level at Pins 5 to 8 is approximately V_B.

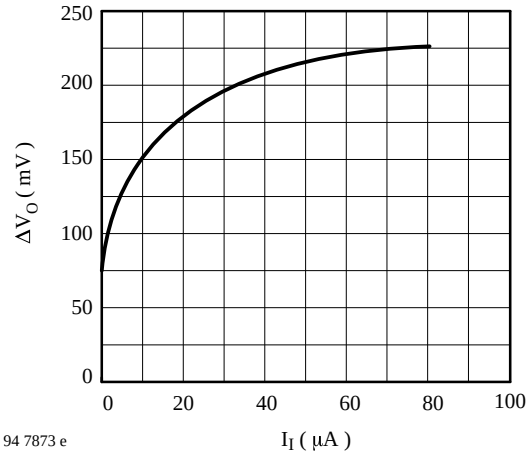


Figure 7.

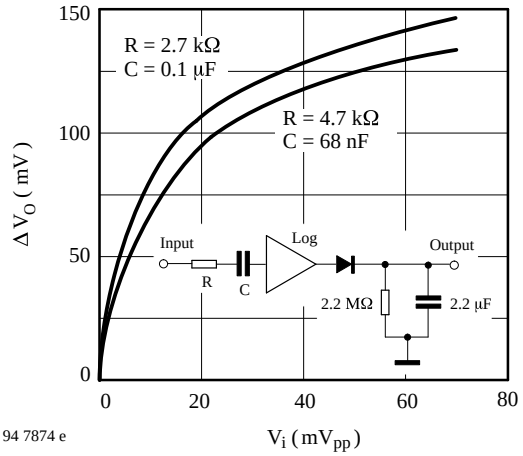


Figure 8.

The T-R comparators responds to the voltages at TLO and RLO, which in turn are functions of the currents sourced out of TLI and RLI, respectively. If an offset at the comparator input is desired (e.g., to prevent noise from switching the system or to give preference to either the transmit or receive channel) it may be achieved by biasing the appropriate input (Pin 5 or 7). A resistor to ground will cause a dc current to flow out of that input, thus forcing the output of that amplifier to be biased slightly higher than normal. This amplifier then becomes the preferred one in the system operation. Resistor values from 500 kΩ to 10 MΩ are recommended for this purpose.

Speaker Amplifier

The speaker amplifier has fixed gain of 34 dB and is non-inverting. The input impedance is nominally 22 kΩ as long as the output signal is lower than required to activate the peak limiter. Figure 9 shows the typical speaker amplifier output (SAO) swing at Pin 15. Since the output current capability is 100 mA, the lower curve is limited to a 5.0 V swing. The output impedance depends on the output signal level and is relatively low when the signal level is lower than the maximum limits. At 3 V_{PP} the output impedance is $\leqq$ 0.5 Ω, and at 4.5 V_{PP} it is $\leqq$ 3 Ω. The output is short-circuit protected at approximately 300 mA.

When the amplifier is overdriven, the peak limiter causes a portion of the input signal to be shunted to ground in order to maintain a constant output level. The effect is that of a gain reduction caused by a reduction of the input impedance at Pin 19 (SAI) to a value not less than 2 kΩ.

The capacitor at Pin 17 (AGC) determines the response time of the peak limiter circuit. When a large input signal is applied to SAI, the voltage at Pin 17 will drop quickly as a current source is applied to the external capacitor.

When the large input signal is reduced, the current source is turned off, and an internal 110 kΩ resistor discharges the capacitor so the voltage at Pin 17 can return to its normal value of 1.9 V dc. The capacitor also stabilizes the peak limiting feedback loop. If there is a need to mute the speaker amplifier without disabling the rest of the circuit, this may be accomplished by connecting a resistor from Pin 17 to ground. A 100 kΩ resistor will reduce the gain by 34 dB (0 dB from SAI to SAO), and a 10 kΩ resistor will reduce the gain by almost 50 dB.

Transmit Detector Circuit

The transmit detector circuit distinguishes speech (which consists of bursts) from the background noise (a relatively constant signal). It does this by storing a voltage level, representative of the average background noise, in the capacitor at CP1 (Pin 11). It has a time constant of approximately 5 seconds (at Pin 11). The voltage at Pin 11 is applied to the inverting input of the transmit detector comparator. In the absence of speech signals, the non-inverting input receives the same voltage level minus an offset of 36 mV. In this condition, the output of the comparator will be low, the the voltage at TDO (Pin 23) will be at ground.

If the T-R comparator is in the transmit position, the attenuator will be in the idle mode (ΔV_{ACF} = 75 mV). When speech is presented to the microphone, the signal burst appearing at TDI reaches the non-inverting input of the transmit detector comparator before the voltage at the inverting input can change, causing the output to switch high, driving the voltage at TDI up to approximately 4 V. This high level causes the attenuator control block to switch the attenuators from the idle mode to the transmit mode (assuming the T-R comparator is in the transmit mode).

As long as the speech continues to arrive and is maintained at a level above the background, the voltage at TDO will be maintained at high level and the circuit will remain in the transmit mode. The time constant of the components at TDO will determine how much time the circuit requires to return to the idle mode after the cessation of microphone speech signals, which occurs during the normal pauses in speech. The series resistor and capacitor at TDI (Pin 13) determine the sensitivity of the transmit detector circuit. Figure 10 indicates the change in dc voltage levels at CP2 and CP1 in response to a steady state sine wave applied at Pin 13 ($\Delta V_{CP1} \approx \Delta$ 2.7 V_{CP2}). Response time can be reduced by increasing the resistor and decreasing the capacitor value at these pins. The first amplifier (between TDI and CP2) regulates a wide range of input signal levels due to AGC. Figure 7 indicates the dc transfer characteristics of the log amp.

Figure 11 shows the following series of events:

1. CP2 (Pin 12) follows the peaks of the speech signals and decays at a rate determined by the 10 µA current source and the capacitor at this pin.
2. CP1 (Pin 11) increases at a rate determined by the RC at this pin after CP has made a positive transition. It will follow the decay pattern of CP2.
3. The non-inverting of the transmit detector comparator follows CP2, gained up by 2.7 and reduced by an offset of 36 mV. This voltage, compared to CP1, determines the output of the comparator.
4. TDO (Pin 23) will rise quickly to 4 V dc in response to a positive transition at CP2, but will decay at a rate determined by the RC at this pin. When TDO is above 3.25 V dc, the circuit will be in the transmit mode. As it decays toward ground, the attenuators are taken to the idle mode.

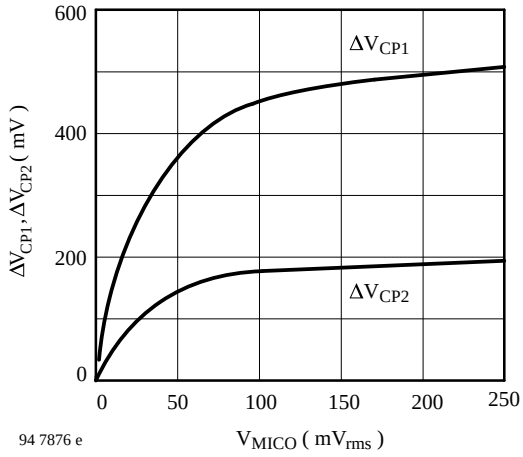


Figure 9.

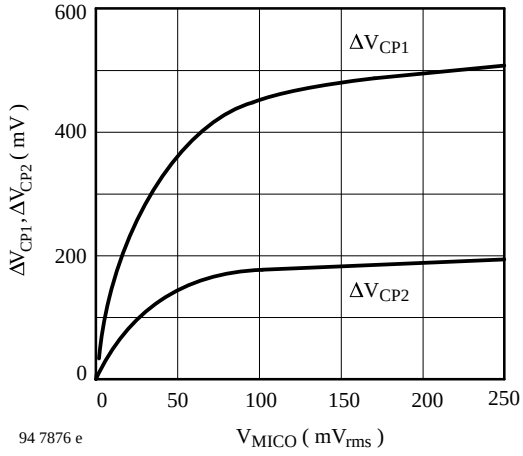


Figure 10.

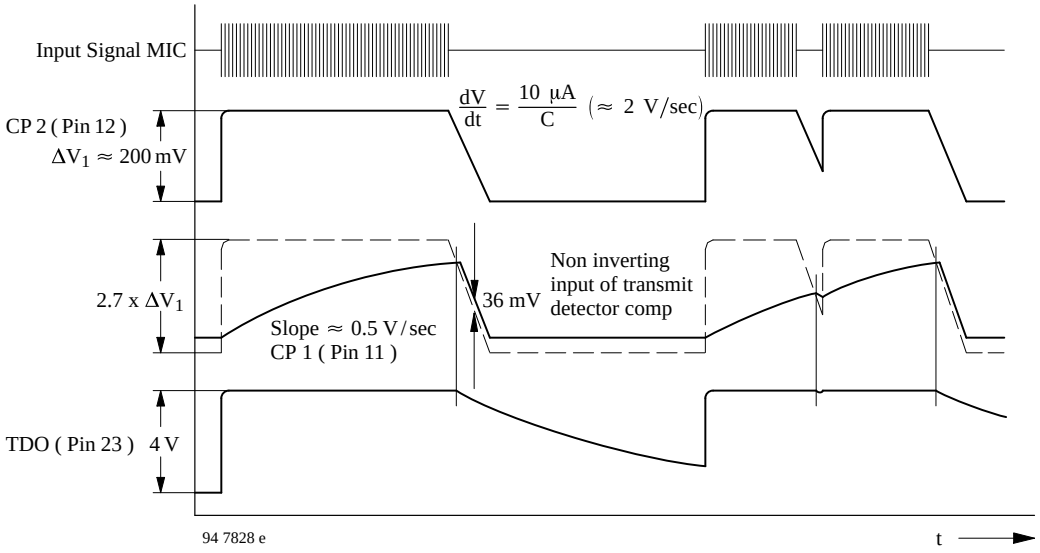


Figure 11. Transmit detector operation

Microphone Amplifier

The microphone amplifier is non-inverting, has an internal gain of 34 dB and a nominal input impedance of 10 kΩ. The output impedance is typically ≦ 15 Ω. The maximum voltage swing available is approximately 2 V less than V_{CC}, which is substantially more than what is required in most applications. The input at Pin 9 (MIC) should be ac coupled to the microphone so as not to upset the bias voltage. Generally, microphone sensitivity may be adjusted by varying the two microphone bias resistors rather than an attempting to vary the gain of the amplifier.

Power Supply (V+)

The voltage for the supply at Pin 16 should be in the range of 6.0 to 11V, although the circuit will operate down to 4.0 V. The voltage can be supplied either from Tip and Ring or from a separate supply. The required supply current, with no signal to the speaker, is shown in figure 12 The upper curve indicates the normal operating current when Chip Select (Pin 18) is a logic O. Figure 13 indicates the average dc current required when supplying various power levels to a 25 Ω speaker. Figure 13 also shows the minimum supply voltage required to provide the indicated power levels. The peak in the power supply current at 5.0 to 5.4 V occurs as the V_{CC} circuit comes into regulation.

For stability reasons, supply should be grounded properly against ac noise. If this pin is not well filtered (by a 1000 µF capacitor), any variation at V+ caused by the required speaker current flowing through this pin can cause a low frequency oscillation. The result is usually that the circuit will cut the speaker signal on and off at the rate of a few hertz. Experiments have shown that only a few inches of wire between the supply and the IC can cause the problem if the filter capacitor is not physically adjacent to the IC. It is equally imperative that both ground pins (Pins 14 and 22) have a loss connection to the power supply ground.

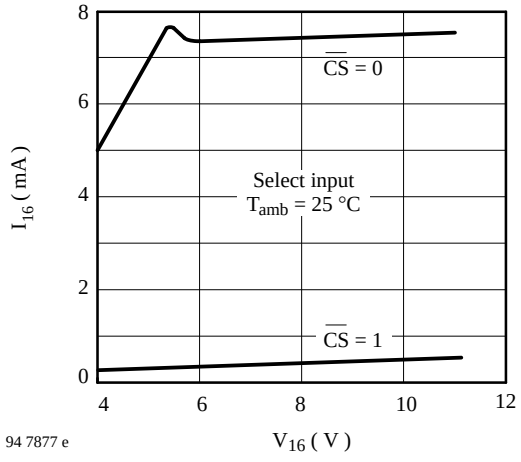


Figure 12.

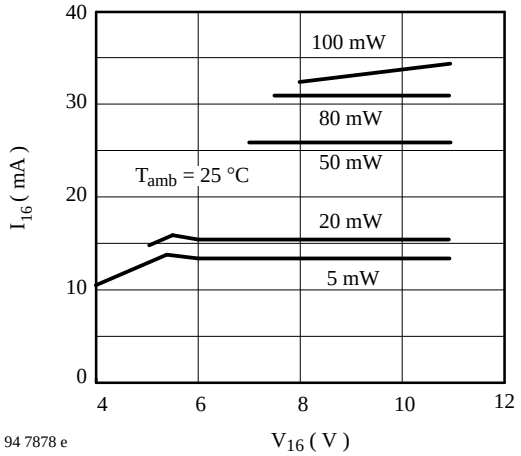


Figure 13.

V_{CC} (Pin 20) is a regulated output voltage of 5.4 V ± 0.5 V. Regulation will be maintained as long as V+ is (typically) 80 mV greater than the regulated value of V_{CC}. Up to 3 mA can be sourced from this supply for external use. The output impedance is ≦ 20 Ω. The 47 µF capacitor indicated for connection to Pin 20 is essential for stability reasons. It must be located adjacent to the IC.

If the circuit is deselected (see the section on chip select), the V_{CC} voltage will go to 0 V.

If the integrated circuit, U4080B, is to be powered from a regulated supply (not the Tip and Ring lines) of less than 6.5 V, the configuration of figure 14 may be used so as to ensure that V_{CC} is regulated. The regulated voltage is applied to both V+ and V_{CC}, with CS held at a logic 1 so as to turn off the internal regulator (the Chip Select function is not available when the circuit is used in this manner). Figure 15 indicates the supply current by this configuration, with no signal at the speaker. When a signal is sent to the speaker the curves of figure 13 apply.

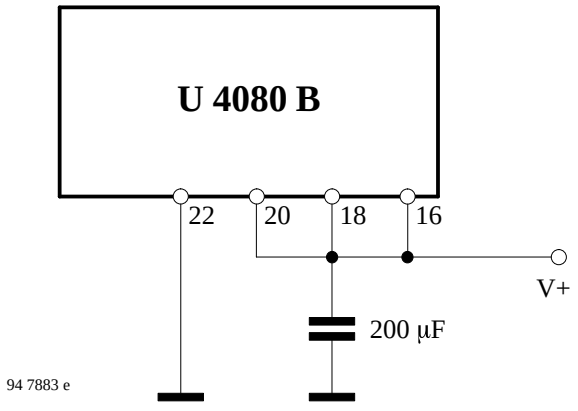


Figure 14. Regulated power supply

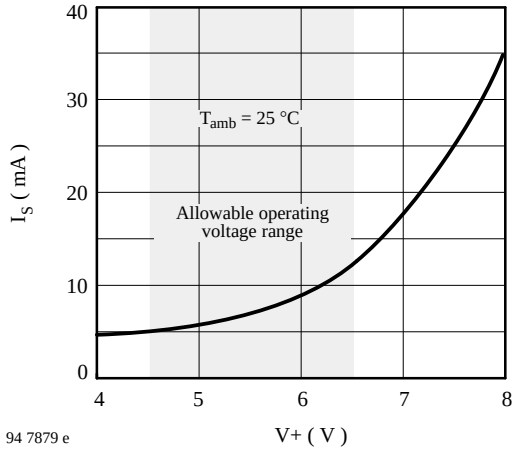


Figure 15.

V_B

V_B is a regulated output voltage with a nominal value of 2.9 V ± 0.4 V. It is derived from V_{CC} and tracks it, holding a value of approximately 54% of V_{CC}. 1.5 mA can be sourced from this supply at a typical output impedance of 250 Ω. The 47 µF capacitor indicated for connection to the V_B pin is required for stability reasons, and must be adjacent to the IC. If the circuit is deselected (see section on chip select), the V_B voltage will go to 0 V.

Chip Select

The Chip Select pin (Pin 18) allows the chip to be powered down anytime its functions are not required. A logic 1 level in the range of 1.6 to 11 V deselects the chip, and the resulting supply current (at V+) is shown in figure 12 The input resistance at Pin 18 is ≧ 75 kΩ. The V_{CC} and the V_B regulated voltages go to zero when the chip is deselected. Leaving Pin 18 open is equivalent to a logic O (chip enabled).

Switching time

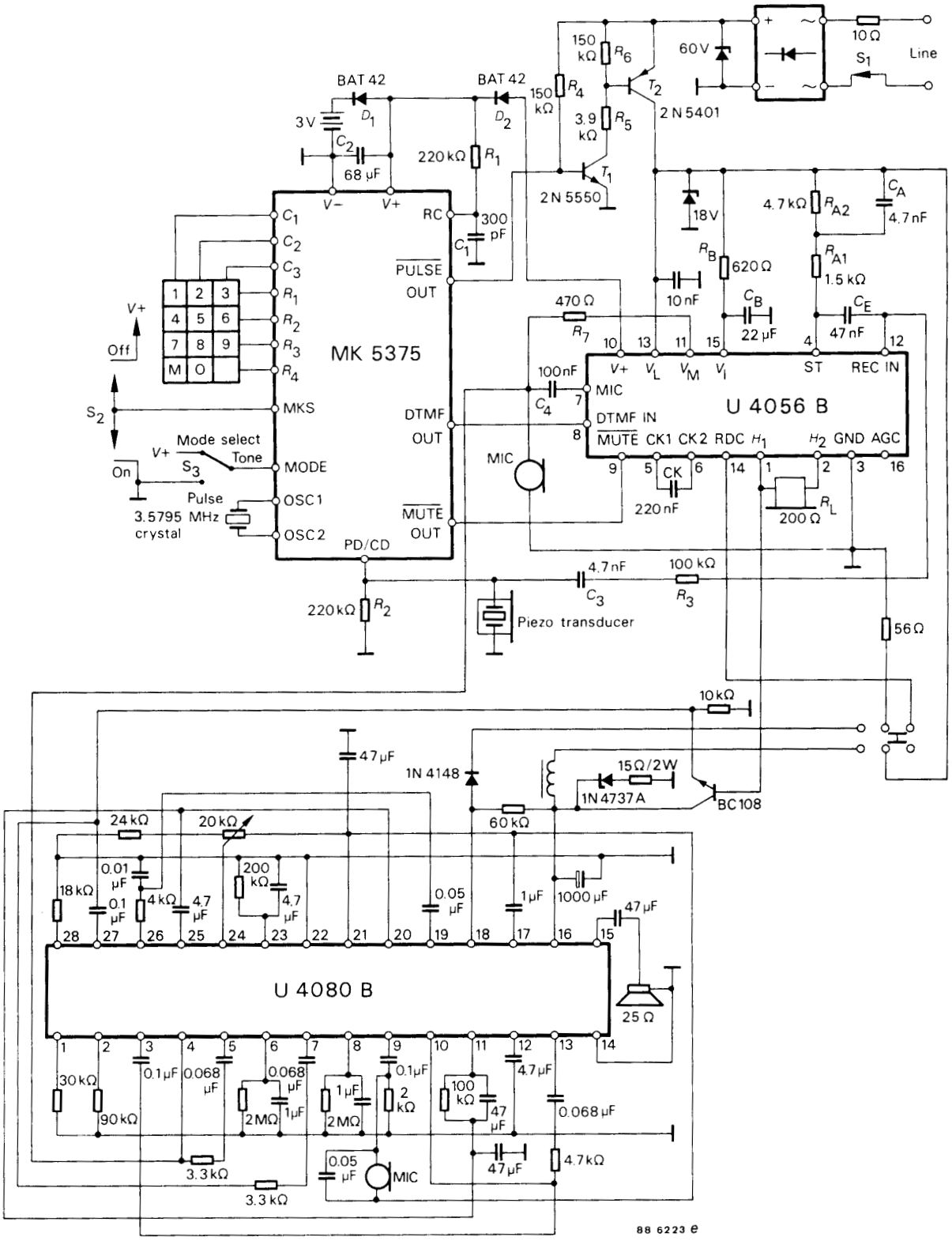
The switching times of the speakerphone circuit depend not only on the various external components, but also on the operating condition of the circuit at the same time a change is to take effect. For example, the switching time from idle to transmit is generally quicker than the switching time from receive to transmit (or transmit to receive).

The components which most significantly affect the timing between the transmit and receive modes are those at Pin 5 (transmit turn-on), Pin 6 (transmit turn-off), Pin 7 (receive turn-on), and Pin 8 (receive turn-off). These four timing functions are not independent, but interact since the T-R comparator operates on a relative T-R comparison, rather than on absolute values. The components at Pins 11, 12, 13 and 23 affect the timing from the transmit to the idle mode. Timing from the idle mode to transmit mode is relatively quick (due to the quick charging of the various capacitors), and is not greatly affected by the component values. Pins 5–8 do not affect the idle-to-transmit timing since the T-R comparator must already be in the transmit mode for this to occur.

Additionally, the following should be noted:

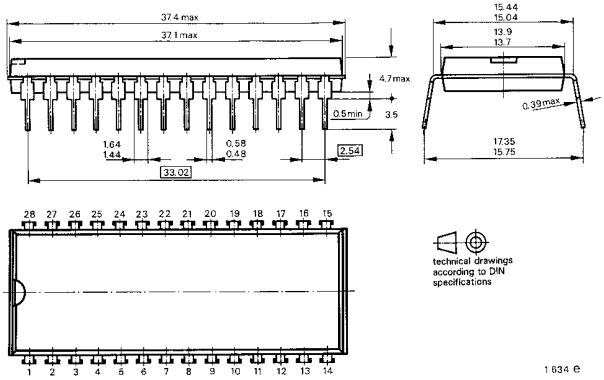
1. The RC circuits at Pins 5 and 7 have dual function in that they affect the sensitivity of the respective log amplifiers or in other words, how loud the speech must be in order to gain control of the speakerphone circuit.
2. The RC circuit at Pin 13 also has a dual function in that it determines the sensitivity of the transmit detector circuit.
3. The volume control affects the switching speed and the relative response to transmit signals in the following manner:
   When the circuit is in the receive mode, reducing the volume control setting increases the signal at TO, and consequently the signal to the TLI pin. Therefore, a given signal at TI will switch the circuit into the transmit mode quicker at low volume settings.

Application



Dimensions in mm

Package: DIP 28



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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